GRSCRUB ADA-SDEV-KIT2 Demo

1.0 OVERVIEW

This document describes the setup demonstrating the Cobham Gaisler's GRSCRUB IP functionalities targeting the Kintex Ultrascale FPGA on the ADA-SDEV-KIT2 development board.

2.0 INTRODUCTION

The Cobham Gaisler's GRSCRUB IP is an external FPGA configuration supervisor that features programming and scrubbing capabilities, which prevents the accumulation of errors in the configuration memory of SRAM-based FPGAs. The GRSCRUB IP is able to detect and correct single and multiple errors affecting the FPGA configuration memory. The GRSCRUB IP is currently compatible with the Kintex UltraScale and Virtex-5 Xilinx FPGA families. The configuration memory of the target FPGA is accessed externally through the slave SelectMap (SMAP) configuration interface.

The GRSCRUB IP scrubbing supports both blind and readback scrubbing methods. The error detection in readback scrubbing can be performed by Full Frame Check (FFC), which verifies all bits of the FPGA configuration frames, or using a standard 32-bit CRC algorithm, which verifies the CRC code of each configuration frame.

3.0 EVALUATION TEST SETUP

The evaluation setup consists of a test controller FPGA embedding the GRSCRUB IP and the target FPGA under evaluation. Fig. 1 presents the block diagram and the experimental setup of the tests. The test controller is a Xilinx KCU105 evaluation board featuring a Xilinx Kintex UltraScale XCKU040 FPGA. An AlphaData ADM-SDEV-BASE development kit embedding a Xilinx Kintex UltraScale XCKU060 FPGA is the adopted target FPGA.

Two FPGA Mezzanine Card (FMC) breakout boards are used to allow the communication between the test controller and the target FPGA. The FMC cards were adapted to access the SelectMap signals of the target FPGA, which are connected to the Config FMC Socket (J2) of the AlphaData ADM-SDEV-BASE board.

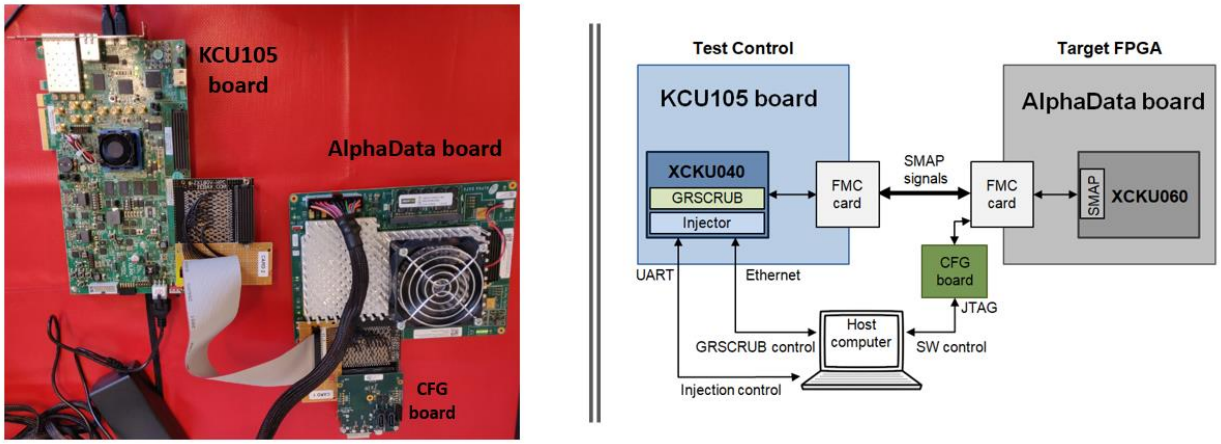

Fig. 1. GRSCRUB IP evaluation test setup.

4.0 DESIGN UNDER TEST

Besides the GRSCRUB IP, the test controller implements a fault injection engine that emulates faults on the configuration memory of the target FPGA. The test controller design also contains other IP cores from the GRLIB IP library, such as the AHB bus, DDR3 memory controller, Debug Support Unit (DSU), Ethernet, and UART. In this setup, the GRSCRUB IP is controlled through Ethernet using Cobham Gaisler's GRMON3 debug monitor.

Two test designs were implemented in the target FPGA for the evaluation experiments:

- **Static design:** the design does not implement any dynamic function, and therefore most of the configuration bitstream is empty. The functionality of the design is not evaluated since the goal is only to validate the GRSCRUB IP features. The fault injection targets all FPGA configuration frames, and the IP also monitors the entire configuration memory.

- **LEON3FT-based design:** the design implements a LEON3FT processor core. In addition to the LEON3FT processor, the design also contains other IP cores from GRLIB [6], such as DSU, fault-tolerant SRAM module, AHB bus, JTAG, and UART. The floorplanning of the design is constrained to a specific area, and both fault injection and GRSCRUB IP only target this area.

5.0 EVALUATION RESULTS

The blind, readback FFC, and readback CRC scrubbing modes of the GRSCRUB IP were evaluated by fault correction capability with faults affecting the Static design implemented in the target FPGA. Single or multiple random faults were injected per run, and then the GRSCRUB IP scrubbing mode was enabled to correct the faults. More than 350 thousand faults were injected into the target FPGA configuration memory. In all tests, the GRSCRUB IP was able to detect and correct all injected faults.

The tests with the LEON3FT-based design implemented in the target FPGA demonstrated that 99.6% of the software runs were successful. The software was executed continuously while single random faults were injected in the target FPGA. After each injection, the GRSCRUB IP readback FFC scrubbing was enabled to clear the fault. A total of 11,399 faults were injected, and the GRSCRUB IP was able to correct all injected faults.

6.0 CONCLUSION

The Cobham Gaisler's GRSCRUB IP is an FPGA configuration supervisor that features programming and scrubbing capabilities. Fault injection tests targeting the Xilinx Kintex UltraScale FPGA embedded in the AlphaData ADM-SDEV-BASE board demonstrated the GRSCRUB IP capability to correct all injected faults in the FPGA configuration memory. Tests in a LEON3FT design confirm that the GRSCRUB IP scrubbing operation allows uninterrupted software execution in the presence of correctable errors in the FPGA configuration memory by preventing the error build-up. The GRSCRUB IP minimizes the latency of single points of failure in the system, but it does not avoid errors happening and neither their effects on the design. Additional mitigation techniques at the design level are recommended to decrease the number of single points of failure and increase the fault masking.

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